Attorney Docket No. 0756-7660

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2893
Kiyoshi KATO et al.	)	Examiner: E. Woldegeorgis
Serial No. 10/573,527	)	
Filed: March 24, 2006	)	
For: MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 30, 2009.

RESPONSE

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Official Action mailed October 30, 2008, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statement filed on March 24, 2006.

Claims 1-16 are pending in the present application, of which claims 1, 4, 7, 11 and 15 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 5 of the Official Action rejects claims 1-16 as anticipated by U.S. Publication No. 2005/0174845 to Koyama. The Applicant respectfully traverses the rejection because the Official Action has not established an anticipation rejection.

As stated in MPEP § 2131, to establish an anticipation rejection, each and every element as set forth in the claim must be described either expressly or inherently in a

single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The Applicant respectfully submits that an anticipation rejection cannot be maintained against the independent claims of the present application. Independent claims 1, 4, 7, 11 and 15 recite that a semiconductor film interposed between two wirings of a memory cell is altered by applying a voltage between an electrode and at least one of the two wirings. For the reasons provided below, the Applicant respectfully submits that Koyama does not teach the above-referenced features of the present invention, either explicitly or inherently.

The Official Action asserts that "Koyama ... discloses (Figure 15) a memory device comprising a memory cell ... formed over an insulating surface (3000), which includes a semiconductor film (3003) having two impurity regions (3014/3015, Par [0120]), a gate electrode (3007/3011), and two wirings (3026/3027) connected to the respective impurity regions (3014/3015, Par [0120]), wherein the semiconductor film (3003) interposed between the two wrings (3026/3027) of the memory cell ... is altered by applying a voltage (Par [0085]) between the gate electrode (3007/3011) and at least one of the two wirings (3026/3027)" (page 3, Paper No. 20080916; emphasis added). Also, in addition to Figure 15, the Official Action cites Figures 22A-23I and paragraph [0085] in the rejection of independent claims 4, 11 and 15 and paragraph [0019] in the rejection of claim 7. The Applicant respectfully disagrees and traverses the assertions in the Official Action.

Paragraphs [0019] and [0085] of Koyama, while generally referring to blowing a fuse element, do not appear to specifically disclose that a semiconductor film interposed between two wrings of a memory cell is altered by applying a voltage between a gate electrode and at least one of two wirings. The Applicant respectfully submits that these features are not taught, either explicitly or inherently, in Koyama, including the disclosure of paragraphs [0019] and [0085] and Figures 15 and 22A-23I.

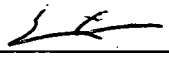
Therefore, the Applicant respectfully submits that Koyama does not teach that a semiconductor film interposed between two wirings of a memory cell is altered by applying a voltage between an electrode and at least one of the two wirings, either explicitly or inherently.

Furthermore, claims 1 and 4 recite "a semiconductor film having two impurity regions." Claims 7 and 11 recite "a semiconductor film having one or two impurity regions." The Official Action asserts that the first impurity region 3014 and 3015 in Koyama correspond with "two impurity regions" in the rejection of claim 1 (page 3, Paper No. 20080916) and as "one or two impurity regions" in the rejection of claim 7 (page 4, Id.). Similarly, the Official Action asserts that the low concentration impurity regions 65 and the high concentration impurity regions 68 correspond with "two impurity regions" in the rejection of claim 4 (page 3, Id.) and as "one or two impurity regions" in the rejection of claim 11 (page 5, Id.). These assertions appear to be contradictory, and the Applicant respectfully submits that Koyama fails to teach both one and two impurity regions as presently claimed.

Since Koyama does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102 are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789